A Chip-First Approach to Millimeter-Wave Circuit Packaging

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***Abstract*— In this letter, we demonstrate a fully additively manufactured packaging solution for the integration of millimeter-wave (mm-wave) devices. This technique employs a chip-first approach to packaging, where die and other components are positioned and a package and interconnects are subsequently built up. This letter allows for the dense populations of components even when they do not share a common vertical height. To demonstrate this concept, we present the fabrication and measurement of two packaged 0-dB attenuators to characterize the performance of the interconnect strategy. These interconnects achieve a worst case loss of 0.290 dB at 40 GHz. Beyond the rated operating range of the device, which is from dc to 43.5 GHz, the interconnects achieve a worst case loss of 0.490 dB at 60 GHz. The approach that we present provides a flexible mm-wave capable and broadband packaging solution that enables the next-generation system-in-package technology.**

***Index Terms*— Additive manufacturing (AM), aerosol jet printing (AJP), millimeter-wave (mm-wave) interconnect, system-in-package.**

I. Introduction

THE demand for millimeter-wave (mm-wave) electronics has continued to steadily rise, and there is no indication that this trend will cease. While many applications have been proposed or demonstrated in imaging, sensing, radar, and communications, new packaging and interconnect strategies must be developed to meet the performance demands of these mm-wave applications. Conventional methodologies typically use wire bonds to form interconnects between the chip and the board. Wire bonds become an increasingly difficult design constraint as operating frequencies increase. The large inductive discontinuity they present to signal paths becomes detrimental to performance. While the mm-wave performance can be achieved with wire bonds, it is typically achieved over narrow bandwidths using matching networks [1]. For many applications, this is unacceptable. Flip chip methods can provide mm-wave and broadband interconnects as demonstrated in [2], but require strict mechanical constraints in their practical implementation and risk parasitic detuning.

Additive manufacturing (AM) may provide a viable solution for the packaging of mm-wave electronics. Many others have demonstrated mm-wave and RF electronic components manufactured with AM technologies [3], [4]. This letter has focused on passive structures, such as antennas, waveguides, and filters. AM is an attractive solution to the fabrication of mm-wave and RF components and systems, as it is a flexible design platform. With AM techniques, structures need not be limited to a flat plane, and the technology is capable of tailoring a design to a specific application. Furthermore, AM may be a more efficient means of producing integrated electronics, requiring fewer chemical and specialized processes associated with the state-of-the-art board manufacturing.

The prospect of building packaging and interconnects using AM, and specifically the so-called direct write technologies, such as aerosol jet printing (AJP) or inkjet printing, was demonstrated in [5], [6], and references therein. A demonstration of such an interconnect approach for mm-wave applications was shown in [7] up to 40 GHz on a blank die, which demonstrated interconnects built with a dielectric ramp up to a chip. In this letter, we show a mm-wave interconnect, which incorporates a printed dielectric package around a commercial-off-the-shelf (COTS) GaAs mm-wave component. Furthermore, we demonstrate interconnects operating up to 67 GHz, as well as an order of magnitude improvement on the loss performance of the interconnect compared with the previous reports. This is an extension of this letter in [8], thus improving both the frequency performance and loss of our chip-first approach to packaging. Reference [8] used a similar strategy with a silicon COTS die only to 20 GHz, and the results showed about twice as much loss as is shown in this letter.

II. Design

The design of this package is simple and flexible. The package that we demonstrate consists of a printed dielectric around a COTS component. We used a 0-dB GaAs attenuator, KAT-0-DG+, manufactured by Mini-Circuits, which has an operational frequency range of 0–43.5 GHz and is 100 μm thick. The conductors consist of printed conductor-backed coplanar waveguides (CPWG) to facilitate measurements, transitions to microstrip (MS) structures, and an interconnect region. The design is implemented on a copper plate with a printed polyimide ($\epsilon_r \approx 3.5$). We designed the transition region between CPWG and MS as outlined in [9] with additional grounding straps to the copper substrate for the improved low-frequency performance. The copper substrate serves as a ground for the MS waveguide. The package is designed to operate in a 50-Ω environment. The details of the design are shown in Fig. 1.

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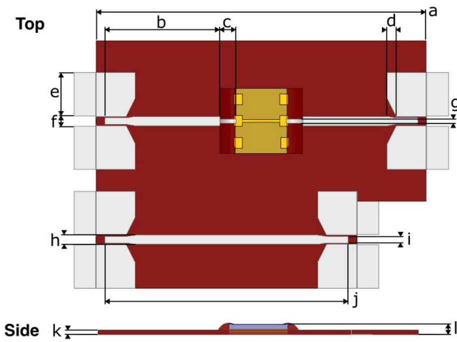

Fig. 1. Designed part (in units of mm) a) package length = 3.7, b) printed signal length = 1.25, c) inductive signal length = 0.184, d) CPWG to MS transition length = 0.1, e) probe ground width = 0.505, f) CPWG ground to ground space = 0.107, g) inductive signal width = 0.048, h) MS width = 0.108, i) CPWG signal width = 0.075, j) 2× through trace length = 2.4, k) package height = 0.05, and l) mounted die height = 0.125.

At the device, the bonding pad presents a capacitive discontinuity. This discontinuity would typically be insignificant compared with the discontinuity created by a bond wire interconnect. A narrower inductive section is introduced in series with the printed MS to compensate for the capacitance of the pad to improve the impedance matching. The length of the interconnect region is approximately 0.06 λ long at 67 GHz, so it acts as a lumped element. We optimized this region in simulation using ANSYS HFSS. Our approach does not require large bond pads on the device, but COTS mm-wave frequency components are not available with small bond pads. This stepped impedance compensation is similar to how inductive bond wires are compensated, but this design is much broader band because the discontinuity presented by the capacitive pad is smaller than the inductive discontinuity that a bond wire presents.

III. Fabrication

Unlike other mm-wave packaging strategies which first form a cavity in which a die is placed, our strategy uses a chip-first approach. The die is placed on a substrate, and then, a package and interconnects are built around them. This strategy is not sensitive to die placement since the printer can be aligned to the die and corrected for misalignment. The dielectric thickness can also be tailored to individual dies. We fabricated the printed package and interconnects using the AJP technology with an Optomec Aerosol Jet 5x printer. AJP deposits the material contained in a focused aerosol stream. This manufacturing process allows for the printing of the material at standoff heights as great as 10 mm while maintaining the minimum printed feature sizes below 10 μm. Owing to the large standoff, many components can be packaged simultaneously even when their bonding surfaces are at different relative heights. The minimum line space with this approach is 10 μm, meaning that a line pitch of 20 μm is achievable. Therefore, this packaging approach is scalable to higher density packaging applications.

We placed the die on a copper substrate using Ablebond 84-1LMISR4 conductive epoxy. The dielectric printing was performed in two steps using polyimide precursor ink composed of 15% wt. polyamic acid in N-methyl-2-pyrrolidinone (NMP) manufactured by Sigma Aldrich diluted to 5% wt. in NMP. Our design assumes $\epsilon_r = 3.5$ and $\tan\delta = 0.008$. First, we printed at 75° relative to the surface of the copper-polyimide ink around the sides of the device and along the edge of the die surface to cover the conductive sealing ring around the edge of the die. Second, we printed the package around the die to a target thickness of 50 μm at 90° relative to the surface of the copper. The printing stage was heated to 100 °C to dry the ink as it was printed, allowing thick films to be deposited without curing the ink after every layer. Polyimide was printed using a 300-μm nozzle with an aerosol flow rate of 25 SCCM. We heat-cured (imidized) the polyimide ink after each of these two steps. Finally, we printed conductive interconnects on a cured polyimide using Clariant Prelect TPS 50 silver nanoparticle ink using a 100-μm nozzle and an aerosol flow rate of 20 SCCM. On a representative sample of cured printed silver ink on polyimide, we achieved 53% of the bulk conductivity of silver (a resistivity of 3×10^{-6} Ω-cm), measured with a Lucas Labs Pro4 four-point resistivity system.

We fabricated two identical packages with 23 layers of polyimide ink and three layers of silver ink. We measured the thicknesses of the polyimide packages–dimension k in Fig. 1– with a NanoMap-500LS Surface Profilometer to be 40.9 μm (Package I) and 51.04 μm (Package II) with an rms surface roughness of 0.5 and 0.3 μm, respectively. Similarly, we measured the silver layers to be 5.1 and 5.2 μm thick with an rms surface roughness of 0.7 and 0.4 μm, respectively. One of the fabricated parts is shown in Fig. 2.

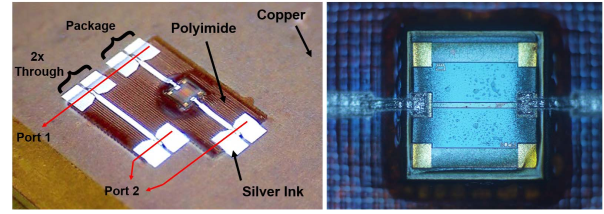

Fig. 2. One of the two identical fabricated packages and 10× magnified detail of interconnects.

IV. Results

We took measurements with an MPI TS150-THZ Probe System and a Keysight N5227 PNA. After short-open-load-through calibration, the reference plane of the measurements is moved to the tips of the ground-signal-ground (GSG) probes. The measured and simulated S-parameters are shown in Fig. 3. The difference between the two measured packages is due to the landing position of the GSG probes on the CPWG launch and deviation in the dielectric thickness. Both samples maintained reflections ≤ -10 dB to beyond 55 GHz. The surface roughness of the printed conductors is likely the reason for higher losses with increasing frequency than predicted by the simulation. Using the simultaneously fabricated 2× through calibration line and the measured die alone (unpackaged), the loss of the interconnects alone can be determined by $S^i_{21} = (S^m_{21} - S^t_{21} - S^d_{21})/2$, where S^i_{21}, S^m_{21}, S^t_{21}, and S^d_{21} represent the loss of a single interconnect, the measured loss of the entire package, the measured loss of the 2× through calibration line, and the measured loss of the die, respectively.

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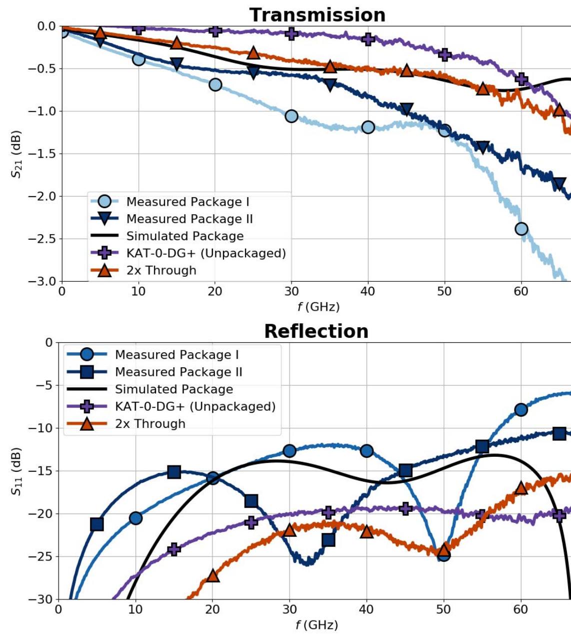

Fig. 3. Measured and simulated scattering parameters of the two identical measured packages, the simulated performance of these packages, the measured unpackaged attenuator, and the printed 2× through line.

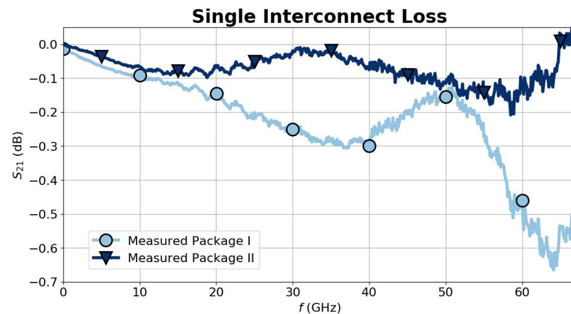

Fig. 4. Calculated loss of a single interconnect (0.234 mm long).

Fig. 4 shows the loss of the interconnects alone. The effective length of each interconnect is 0.234 mm, found by the printed signal length minus half of the 2× through the length plus the inductive signal length. The difference in loss between the two packages is less than 0.62 dB over the range of measurement and less than 0.28 dB over the operating range of the attenuator. At approximately 65 GHz, above the operating frequency of the device, nonpassivity errors exist in the calculated loss with magnitudes $\leq$0.07 dB. These errors can be accounted for by differences in the magnitude of the reflection between the calibration trace and the measured packaged device and by variability in the performance of the probe launch at these frequencies. The losses of the interconnects presented here are an order of magnitude better than any previously published work. The interconnect loss of this letter at 20 GHz including the transmission line is comparable to the loss in [8] at 20 GHz, 0.289 and 0.209 dB, but the package presented here is 1 mm shorter. This letter extends the usable frequency range of our previously published work from 20 to 67 GHz. These results are better than our previous work for three reasons: first, the interconnect region is shorter; second, the probe launch is better designed and the capacitive bond pad is compensated for and so mm-wave performance is improved; and third, the silver layer is thicker and achieves a higher conductivity. A thicker silver lowers the loss from the skin effect. A comparison of the best reported AM mm-wave and Ku-to-Ka band interconnect performance is shown in Table I. Future work in this area should study the long-term reliability of this style of packaging.

TABLE I
COMPARISON OF AM HIGH-FREQUENCY (SINGLE) INTERCONNECTS

	This Work	[8]	[7]	[10]
AM Technology	**AJP**	AJP	Inkjet	AJP
Die	**COTS GaAs**	COTS Si	Blank Si	PCB
S_{21} (20 GHz)	**-0.146 dB**[a]	-0.22 dB	$\approx$ -1.5 dB	$\approx$ -1.3 dB[b]
S_{21} (40 GHz)	**-0.290 dB**[a]	n/a	$\approx$ -1.6 dB	n/a
S_{21} (60 GHz)	**-0.490 dB**[a]	n/a	n/a	n/a

[a]Worst case of two samples, [b]May include PCB loss of die stand-in

V. CONCLUSION

Our chip-first packaging methodology is fully additively-manufactured and mm-wave capable. The results of this letter improve on the previously published mm-wave interconnect loss performance by an order of magnitude. Using an AM packaging approach, a 200% fractional bandwidth, low-loss interconnect can be fabricated, which is not realizable with bond wire interconnects. This flexible approach to packaging shows potential for enabling the next-generation system-in-package technology integration.

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